ABSTRACT

After forming a silicon oxide film 9 on the surface of a region A of a semiconductor substrate 1, a high dielectric constant insulating film 10, a silicon film, a silicon oxide film 14 are successively deposited over the semiconductor substrate 1, and they are patterned to leave the silicon oxide film 14 in regions for forming gate electrodes. Then, after fabricating silicon films 13n and 13p by using the patterned silicon oxide film 14 as a mask, when removing the silicon oxide film 14, etching is performed under the condition where the etching selectivity of the silicon oxide film 14 to the high dielectric constant insulating film 10 becomes large, thereby leaving the high dielectric constant insulating film 10 also to portions below the end of the gate electrodes (13n, 13p). Thus, it is possible to ensure the voltage withstanding thereof and improve the characteristics of MISFET.